

Reliability Evaluation Report

MDG–MCD–RER 1911

STM32F/STM32L/ STM8L (438–425–444–761)

WBC to DAF for UQFN4x4 COL 28L & UQFN5x5 COL32L

JSCC (PCN11503)

General Information		Traceability	
Commercial Product	STM32F334K8U6 STM32L031G6U6 STM32F031G6U6 STM8L101G2U6	Diffusion Plant	Rousset RS8F TSMC FAB 3 – FAB11
Product Line	438X66, 425X66, 444X66, 761X19	Assembly Plant	JSCC – CHINA
Die revision	X438XXXZ, X425XXXX, X444XXXA, 761XXX		
Product Description	STM32F, STM32L, STM8L		
Package	UQFN5x5 COL 32L (Chip On Lead) UQFN4x4 COL 28L (Chip On Lead)	Reliability Assessment	
Silicon Technology	CMOSF9S–CMOSF9GO2 RS8F, 0.18 TSMC	Pass	<input checked="" type="checkbox"/>
Division	MDG–MCD	Fail	<input type="checkbox"/>

Note: this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).

Version	Date	Author	Function
1.0	Nov 02nd 2020	Bambang Redjeki SIE Céline Navarro	MDG–Q&R MDG–MCD–Q&R

APPROVED BY:

Function	Location	Name	Date
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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation performed on STM8L, STM32L, STM32F for UQFN4x4 COL and UQFN5x5 COL WBC (wafer back-side coating) to DAF (die attach film).

This Production Change Notification (PCN) concerns change of WBC to DAF for UQFN4x4 COL and UQFN5x5 COL at JSCC China.

Changes are described here below:

	From:	To:
Assembly site	JSCC (China)	JSCC (China)
Die Attach material	WBC Epoxy Henkel 8006NS	DAF Hitachi HR-5104T-25

1.2 Reliability Strategy

4 Test vehicles for reliability trials are described here below:

Product	Process or Package	Diffusion or Assembly plant
STM32F334K8U6	0.18EMBF/2P – QFN5X5 COL 32L x 0.5	TSMC – JSCC
STM32L031G6U6	CMOSF9S-5M – QFN4x4 COL 28L x 0.55	RS8F – JSCC
STM32F031G6U6	0.18EMBF/2P – QFN4x4 COL 28L x 0.55	TSMC – JSCC
STM8L101G2U6	CMOSF9-G02 – QFN4x4 COL 28L x 0.55	RS8F – JSCC

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard.

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results and reliability strategy, the qualification is granted for MCD devices with DAF in UQFN COL.

Refer to Section 3.0 for reliability test results.

2 TEST VEHICLE CHARACTERISTICS

2.1 Generalities

Package line	Assembly Line Package	Device (RawLine Code)	Diffusion Process	Number of Lots
QFN	QFN 5X5x0.5 COL 32L	81EL*438ESXZ	0.18EMBF/2P	1
	QFN 4x4x0.55 COL 28L	83MB*425ESXX	CMOSF9S–5M	1
	QFN 4x4x0.55 COL 28L	85MB*444ESXA	0.18EMBF/2P	1
	QFN 4x4x0.55 COL 28L	80MB*761ESXY	CMOSF9–G02	1

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information				
Test vehicle	438	425	444	761
Wafer fab name / location	TS3F TSMC	RS8F Rousset	TS3F TSMC	RS8F Rousset
Wafer diameter	8 inches			
Wafer thickness	381 +/- 25µm	375 +/- 25µm	381 +/- 25µm	375 +/- 25µm
Silicon process technology	0.18EMBF/2P	CMOSF9S–5M	0.18EMBF/2P	CMOSF9–G02
Number of masks	33	37	33	39
Die finishing front side (passivation) materials	HDPox 10kA+SRO 1.5kA+PESIN 6kA	USG + NitUV (HFP USG+UV Nitride)	HDPox 10kA+SRO 1.5kA+PESIN 6kA	USG + NitUV (HFP USG+UV Nitride)
Die finishing back side Materials	RAW SILICON – BACK GRINDING			
Die area (Stepping die size)	3914x3760 µm	2132x2528 µm	2458x2360 µm	1256x1788 µm
Die pad size	65x70 µm	53x108 µm	65x70 µm	65x108 µm
Sawing street width (X,Y)	80 x 80 µm			
Metal levels/ Materials/ Thickness	Metal 1 Tin/AlCu/Tin 0.450 µm Metal 2 Tin/AlCu/Tin 0.450 µm Metal 3 Tin/AlCu/Tin 0.450 µm Metal 4 Tin/AlCu/Tin 0.450 µm Metal 5 Tin/AlCu/Tin 0.875 µm	Metal 1 TaN/Ta/Cu 0.280 µm Metal 2 Ti/AlCu/TxTN 0.310 µm Metal 3 Ti/AlCu/TxTN 0.310 µm Metal 4 Ti/AlCu/TxTN 0.310 µm Metal 5 Ti/AlCu/TxTN 1.200 µm	Metal 1 Tin/AlCu/Tin 0.450 µm Metal 2 Tin/AlCu/Tin 0.450 µm Metal 3 Tin/AlCu/Tin 0.450 µm Metal 4 Tin/AlCu/Tin 0.450 µm Metal 5 Tin/AlCu/Tin 0.875 µm	Metal 1 TaN/Ta/Cu 0.280 µm Metal 2 TaN/Ta/Cu 0.350 µm Metal 3 TaN/Ta/Cu 0.350 µm Metal 4 TaN/Ta/Cu 0.350 µm Metal 5 Ti/AlCu/TxTN 0.900 µm

2.2.2 Assembly information

Table 2

Assembly Information die 425, 444, 761	
Assembly plant name / location	JSCC – China
Pitch (mm)	0.5
Die thickness after back-grinding	150 +/- 25µm
Die sawing method	Step cut
Bill of Material elements	
Lead frame material/supplier/reference	QFNs–HD–COL28 4*4 C7NP30*0–572U–STW
Lead frame finishing (material)	e4 Precious metal (Ag, Au, NiPdAu)
Die attach material/type (glue/supplier)	DAF HITACHI HR–5104T–25
Wire bonding material/diameter	GOLD WIRE 0.8 MILS
Molding compound material/supplier/reference	SUMITOMO EME G770HCD
Package Moisture Sensitivity Level (JEDEC J–STD020D)	3
Assembly Information die 438	
Assembly plant name / location	JSCC – China
Pitch (mm)	0.5
Die thickness after back-grinding	150 +/- 25µm
Die sawing method	Step cut
Bill of Material elements	
Lead frame material/supplier/reference	UQFNS–(COL)4S 32L 5x5 C7 NP3 0x0–360U
Lead frame finishing (material)	e4 Precious metal (Ag, Au, NiPdAu)
Die attach material/type (glue/supplier)	DAF HITACHI HR–5104T–25
Wire bonding material/diameter	GOLD WIRE 0.8 MILS
Molding compound material/supplier/reference	SUMITOMO EME G770HCD
Package Moisture Sensitivity Level (JEDEC J–STD020D)	3

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	JSCC (China) / ST Rousset (France)

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link:

http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package
1	CRP645 /#25	Cut1.1	939300721 F0000	81EL*438ESXZ	QFN 5X5x0.5 COL 32L
2	VG92116117/#25	Cut2.2	VG9211611 E0000	83MB*425ESXX	QFN 4x4x0.55 COL 28L
3	9U92704311 /#25)	Cut1.0	9U9270431 S0000	85MB*444ESXA	QFN 4x4x0.55 COL 28L
4	VG8451081Z /#23	Cut 2.2	VG8451082 0000	80MB*761ESXY	QFN 4x4x0.55 COL 28L

3.2 Test plan and results summary

Table 5 – ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESD STM5.3.1	250V 500V 500V 500V	4	3	12	Lot1: 0/3 (die 438) Lot2: 0/3 (die 425) Lot3: 0/3 (die 444) Lot4: 0/3 (die 761)	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3 1	385 462	1617	Lot1: 0/385 Lot2: 0/385 Lot3: 0/385 Lot4: 0/ 462	<i>No delamination TSAM / CSAM after Pre-conditioning</i>
TC	JESD22-A104	Ta=-65/150°C Duration= 1000cyc <input checked="" type="checkbox"/> After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs <input checked="" type="checkbox"/> After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs <input checked="" type="checkbox"/> After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	
AC	JESD 22-A102	168h (121°C/100%RH), 2Atm <input checked="" type="checkbox"/> After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	
bHAST	JESD 22-A110	264h (110°C/85%RH), 2Atm <input checked="" type="checkbox"/> After PC	1	77	77	Lot 4: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 7 – PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including -Wire bond shear -Wire bond pull	ST internal specifications	4	50	150	Lot1: 0/50 Lot2: 0/50 Lot3: 0/50 Lot4 :0/50	CA-04-0120 CA-05-0120 CA-03-0120 CA-28-0720

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress–Test–Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front–End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESD STM5.3.1	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD 22–A108	Temperature, Bias and Operating Life
JESD 22–A103	High Temperature Storage Life
J–STD–020	Moisture/reflow sensitivity classification for non–hermetic solid state surface mount devices
JESD22–A113	Preconditioning of non–hermetic surface mount devices prior to reliability testing
JESD22–A118	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22–A104	Temperature cycling
JESD22–A101	Temperature Humidity Bake
JESD 22–A102	Autoclave
JESD 22–A110	Biased Highly Accelerated temperature & humidity Stress Test

5 GLOSSARY

Reference	Short description
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
AC	Autoclave
ESD CDM	Electrostatic discharge (charge device model)
CA	Construction Analysis

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Céline Navarro / Bambang Redjeki SIE	Initial release	Division Q&R Responsible	RSST	Pascal NARCHE	November 2nd, 2020
			Division Quality Manager	RSST	Gisele SEUBE	November 2nd, 2020

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